

**Please cancel claims 9-20 and add new independent claim 21.**

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1. (Amended) A semiconductor device, comprising:  
a substrate having transistor devices;  
a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias isolated from each other by an air dielectric; and

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a plurality of supporting stubs, each of the plurality of supporting stubs configured to be formed from a same contiguous material, each of the plurality of supporting stubs further configured to form a filled supporting column that extends through the plurality of interconnect levels of the semiconductor device.

2. A semiconductor device as recited in claim 1, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

3. A semiconductor device as recited in claim 1, wherein the plurality of supporting stubs are not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

4. A semiconductor device as recited in claim 1, further comprising:  
a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

5. A semiconductor device as recited in claim 4, wherein the plurality of supporting stubs further support the passivation layer.

6. A semiconductor device, comprising:  
a substrate having transistor devices;  
a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.